29. A system to test a bus comprising:

at least one instruction memory to store a predefined bus stimuli instruction, the predefined bus stimuli instruction representing signals associated with a bus transaction on the bus;

at least one phase generator coupled between the bus and the instruction memory, the at least one phase generator to provide signals to the bus corresponding in response to the predefined bus stimuli instruction.

30. The system of claim 29, wherein the predefined bus stimuli instruction also represents the manner in which the signals are to be transmitted.

Remark

Applicant respectfully requests reconsideration of this application as amended. No claims have been amended or canceled. Therefore, claims 1-30 are now presented for examination.

The undersigned has made repeated attempts to contact the assigned Examiner for this case to set up a telephone interview. Jigar Pancoli was left several messages from 4/17 through 4/27. No response was forthcoming. Ayaz Sheikh, the supervisory Examiner of record was left a message on 5/03. No response was forthcoming. A call to the technology center informed me that the new Examiner on this case was David Wiley. David promptly returned a call I left for him on 5/08 and left a message on my voice mail. Later attempts to contact David have been unsuccessful due to the vacation schedules of both the Examiner and the undersigned.

The undersigned has decided to file the response to final in order to be within the two-month date from the mailing of the final office action. **The undersigned, however, requests that the new Examiner carefully consider the enclosed remark, and call the undersigned if there is anything in the remark to which the Examiner takes exception.** The undersigned is very interested in coming to a final resolution of this application without having to endure a long, drawn out and time consuming appeal.

35 U.S.C. §102 Rejection,

The Examiner has rejected claims 1, 2, 4-6 and 9-30 under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 5,701,409 of Gates. ("Gates").

The Examiner wrote with regard to the applicant's arguments filed on 1/24/00:

> (T)he examiner feels that though the "predefined bus stimuli instruction" might be different then (sic) the error commands of Gates reference, from the claim language, the Gates reference reads on the limitations. A predefined bus stimuli instruction in the examiner's view point, is only a known instruction that causes an action on a bus. The error command is a known instruction that causes an action on the bus.

The undersigned strongly disagrees with the Examiner's assertion that the "predefined bus stimuli instruction" of claim 1 is equivalent to the "error command" of Gates. Further, the applicant asserts that the claim language of claim 1 and other claims clearly indicate this difference. **Claim 1 defines a "predefined bus stimuli instruction" as "representing a bus transaction."** A

"predefined bus stimuli instruction" is **NOT** "only a known instruction that causes an action on a bus" as the Examiner contends. As the Examiner is no doubt aware the applicant is allowed to be his own lexicographer, and the applicant has chosen to define the term "predefined bus stimuli" as written in claim 1. The undersigned respectfully requests that the Examiner respect the applicant's definition as it appears in the claim and not apply his own definition that is contrary to the plain language of the claim.

The term bus transaction is clearly defined in the specification as having "three general stages: the arbitration phase, the address phase, and the data phase." The applicant, as his own lexicographer, is entitled to have this definition applied to the term. The definition of "Bus Transaction" applied by the applicant in the specification is consistent with the meaning of the term as would be understood by someone skilled in the art.

Review of the Gates reference clearly indicates that **the Gate's "error command,"** which the Examiner equates to the applicant's "predefined bus stimuli instruction," **DOES NOT represent a bus transaction.** Rather, Gates teaches, "after a particular **error command** is loaded into the command register of the bus error generation circuit, the bus error generation circuit causes an incorrect parity value to be output onto the PCI bus terminal during a subsequent data write PCI bus cycle" (emphasis added). *See Column 2, Lines 49-53.* Gates does not teach or suggest that the "error command" contains information relating to the arbitration, address and data phases of a bus transaction. In fact, closer

review of the Gates reference indicates that it teaches away from the Examiner's assertion.

The undersigned suggests that the Examiner carefully review Figures 3 & 4, along with the accompanying text in the Detailed description, column 3, line 66 to column 4, line 64. Element 108 of Figure 3 represents the error generation circuit as is described in column 4, line 2 of the detailed description. The only line or signal path passing through the error generation circuit is the normal parity lead 111. Other lines such as the address line 105, which transmits address information, a component of a "bus transaction," does not pass through or originate in the error generation circuit. The command register that the Examiner has equated with the "at least one instruction memory to store the predefined bus stimuli instruction" is contained within that error generation circuit as is shown in Figure 6. *See column 6, lines 10-20 for a description of Figure 6.* It is within this command register that Gates teaches the "error command" is loaded. The question is left for the Examiner to answer: how can the "error command" of Gates be equivalent to a "predefined bus stimuli instruction representing a bus transaction" of claim 1 when the only signal that may be output from the error generation circuit is a parity value and not data, address or arbitration information? As understood by the undersigned the answer is an obvious one: The error command of Gates is not equivalent to the predefined bus stimuli instruction of claim 1, because the Gates does not teach the "error command" as representing a bus transaction.

As is clearly taught in the above referenced section of the Gates Detailed Description, the bus transaction generated during the testing operation is not based on instructions contained within an "error command" stored in an "error command register." *See Column 4, Lines 1-64.*

For clarity and to assist the Examiner in responding to this remark, the applicant has enclosed Figures and portions of the Gates specification, along with portions of the applicant's specification, that have been highlighted for emphasis.

Claim 1 & Dependents Claims 2-14

In order to make a prima facie case of anticipation, the relied upon reference must teach **all** the limitations of the claim. *MPEP 706.02.* **Gates fails to teach the "predefined bus stimuli instruction representing a bus transaction as discussed above.** Accordingly, for at least this reason, claim 1 and all claims dependent there from are in a condition for allowance over Gates.

Additionally, with regard to **dependent claim 2, The command register of Gates,** equated by the Examiner to be equivalent to the "instruction memory" of claim 2, **does not teach to hold a plurality of predefined bus stimuli instructions, or error commands for that matter**. In fact, Gates teaches away from claim 2 by requiring the command register to be cleared after each parity value assertion. *See Column 2, Lines 57-62.* Accordingly, for at least both this reason and the reasons given for claim 1, claim 2 is allowable over the Gates reference.

Claim 15

As discussed above, Gates does not teach an instruction memory for storing a "predefined **sequence** of bus stimuli." Rather, Gates teaches a command register only capable of holding a single error command. The term "sequence" of claim 1 requires that more than one bus stimuli must be stored within the memory.

Claim 16 & dependents 17-20

Claim 16 is a means-plus-function claim and as such, must be interpreted in light of the specification by limiting the scope of the claim to corresponding structure materials or acts contained within the specification. *See MPEP 2181.* In interoperating, claim 16 and its dependents, the Examiner must refer to the specification, and cannot ignore the specification. Accordingly, claim 16 and its dependents are allowable over Gates for at least the same reasons as given above. For instance, the specification discusses the system to a test a bus only in terms of transmitting signals causing the performance of bus transactions, therefore the means plus function claim cannot be without considering such limitations. As discussed, Gates does not teach a "means for storing instructions representing predefined bus stimuli" wherein the bus stimuli cause the performance of bus transactions.

Claim 21 & dependents 22-24

Gates does not teach the "predefined bus stimuli" performing at least one phase of a bus transaction. Gates teaches only that the error generation circuit changes a parity value in certain circumstances. Accordingly, claim 21 is allowable over Gates.

Claim 22

Gates does not teach applying a sequence of bus transactions to a bus as discussed above. Accordingly, for this reason, in addition to the reason given above for claim 21, claim 22 is allowable over the Gates reference.

Claim 25, Claim 29 & Associated dependent claims 26-28 & 30

These claims are allowable for at least the reasons stated above with regard to claim 1. Accordingly, these claims are in a condition of allowance over the Gates reference.

35 U.S.C. §103 Rejection,

The Examiner has rejected claims 3, 7 and 8 under 35 U.S.C. 103 (a) as being unpatentable over Gates.

In order to present a prima facie case of obviousness, the references must teach or suggest all of the claim limitations. For the reasons given above with regard to the 35 U.S.C. 102 rejections above, Gates fails to teach or suggest all the limitations of claims 3, 7 & 8. Accordingly, these claims are in a condition for allowance over Gates.

Conclusion

The undersigned respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, the undersigned respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

The undersigned respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: June 6, 2000

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